Amendment to Claims

1. (original) A method for manufacturing an integrated circuit, the method comprising:

(a) forming a plurality of first conductive gates for nonvolatile memory cells, the first conductive gates being spaced from each other and not electrically interconnected;

(b) forming a plurality of conductive floating gates for the memory cells;

(c) forming a plurality of conductive gate lines each of which provides second conductive gates for one column of the memory cells, wherein the adjacent conductive lines for the adjacent columns are spaced from each other;

(d) forming at least one conductive line electrically interconnecting two or more of the first conductive gates.

2. (original) The method of Claim 1 wherein the first conductive gates are formed before the floating gates and the second conductive gates.

3. (original) The method of Claim 2 wherein the conductive line is formed after the first conductive gates, the floating gates, and the second conductive gates.

4. (original) The method of Claim 1 wherein the conductive line is formed after the first conductive gates, the floating gates, and the second conductive gates.

5. (original) The method of Claim 1 further comprising, after forming the first conductive gates and at least one of the floating gates and the second conductive gates, forming a dielectric to insulate the at least one of the floating gates and the second conductive gates from the conductive line, wherein the dielectric is at least 2000Å thick.

6. (original) The method of Claim 5 wherein the dielectric is at least 3000Å thick.

7. (original) The method of Claim 1 wherein the first conductive gates comprise a semiconductor material, and the conductive line is a metal line.

8. (original) The method of Claim 1 wherein each conductive line interconnects the first conductive gates for at least one row of the memory cells.

9. (original) The method of Claim 1 wherein the conductive gate lines are perpendicular to the conductive lines.

10. (original) The method of Claim 1 further comprising forming substrate isolation regions in the semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

wherein the operation (a) comprises forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure comprises one of the first conductive gates;

wherein the operation (b) comprises:

(b1) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG layer, wherein a maximum distance between points of the adjacent substrate isolation regions above the substrate is not greater than one half of a thickness of the FG layer, and one half of the thickness of the FG layer is smaller than a distance between the adjacent first gate structures; and

(b2) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure.

11. (original) The method of Claim 1 further comprising forming substrate isolation regions in the semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

wherein the operation (a) comprises forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure comprises one of the first conductive gates;

wherein the operation (b) comprises:

(b1) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG layer, wherein the FG layer comprises a planar area between each two adjacent substrate isolation regions and the FG layer comprises a protrusion over each first gate structure; and

(b2) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure.

12-24 (canceled).

25. (currently amended) A method for fabricating an integrated circuit which comprises nonvolatile memory cells, each memory cell having a conductive floating gate and a first conductive gate insulated from each other, the method comprising:

(a) forming substrate isolation regions in a semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

(b) forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure ~~comprising~~ comprises at least one first conductive gate;

(c) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG layer, wherein a maximum distance between points of the adjacent substrate isolation regions above the substrate is not greater than one half of a thickness of the FG layer, and one half of the thickness of the FG layer is smaller than a distance between the adjacent first gate structures;

(d) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure;

(e) forming a plurality of conductive gate lines each of which provides second conductive gates for one column of the memory cells, the second conductive gates being insulated from the floating gates, wherein the adjacent conductive lines for the adjacent columns are spaced from each other.

26. (original) The method of Claim 25 wherein the operation (d) is terminated with reference to a time of detecting that the substrate isolation regions have been exposed.

27. (original) The method of Claim 25 wherein each substrate isolation region traverses an array of the memory cells.

28. (original) The method of Claim 25 wherein first gate structures comprise a dielectric over sidewalls of first conductive gates to insulate the first conductive gates from the floating gates.

29. (original) A method for fabricating an integrated circuit which comprises nonvolatile memory cells, each memory cell having a conductive floating gate and a first conductive gate insulated from each other, the method comprising:

(a) forming substrate isolation regions in a semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

(b) forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure comprising at least one first conductive gate;

(c) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG layer, wherein the FG layer comprises a planar area between each two adjacent substrate isolation regions and the FG layer comprises a protrusion over each first gate structure; and

(d) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure;

(e) forming a plurality of conductive gate lines each of which provides second conductive gates for one column of the memory cells, the second conductive gates being insulated from the floating gates, wherein the adjacent conductive lines for the adjacent columns are spaced from each other.

30. (original) The method of Claim 29 wherein the operation (d) is terminated with reference to a time of detecting that the substrate isolation regions have been exposed.

31. (original) The method of Claim 29 wherein each substrate isolation region traverses an array of the memory cells.

32. (original) The method of Claim 29 wherein first gate structures comprise a dielectric over sidewalls of first conductive gates to insulate the first conductive gates from the floating gates.